Docket No. 243436US2SX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Keitaro IMAI, et al.

SERIAL NO: New Application GAU:

FILED: Herewith EXAMINER:

FOR: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

COPY

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

COPY

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Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
LIST OF REFERENCES CITED BY APPLICANT		243436US2SX	New Application
		APPLICANT: Keitaro IMAI, et al.	COPY
		FILING DATE: Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,153,460	11/28/00	Shigeo OHNISHI, et al.			
	AB	6,459,111	10/01/02	Katsuaki NATORI, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Kinam KIM, "High density stand alone-FRAM: Present and Future", INTEGRATED FERROELECTRICS, Vol. 36, 2001, pgs.21-39
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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STATEMENT OF RELEVANCY

Reference AA on Form PTO-1449:

This publication is referred to in the specification. See page 2, line 16.

Reference AB on Form PTO-1449:

This patent says capacitor structures made by damascene process. Dummy bottom electrode such as $SrPu0_3$ is formed by damascene process with wet etching. The technique suppresses process damage to capacitors.

Reference AW on Form PTO-1449:

$AlrO_3$ encapoulated capacitor and ferroelectric film no-etching processed structure using TiO_2 were presented in this paper. Original papers related to the technique are as follows.

1) Tech. Digest 1997 VLSI Tech Symp . pgs 139-140
2) Proc. SSDM, Tokyo. page 394 (1999)
3) Tech. Digest 2000 VLSI Tech Symp. pgs. 34-35